AMENDMENTS TO THE CLAIMS

Kindly cancel the claims of Groups II and III, namely claims 7-17 and 19-22.

Kindly amend claim 1 as shown in the following listing of claims.

Kindly add new claims 23-26 as shown in the following listing of claims.

The following listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

Claim 1 (currently amended): A method of programming a memory array that comprises a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a channel and being programmable using channel hot electron injection, the method comprising:

applying a first voltage to the channels;

generating ~~establishing a voltage differential across the respective channels of at least a first and a second of the memory cells, the potential differential being sufficient to generate~~ channel hot electrons in the ~~respective~~ channels ~~thereof~~ of at least a first and a second of the memory cells;

applying a second voltage to the gate of the first memory cell, the second voltage having a polarity and magnitude relative to the first voltage sufficient to attract the hot electrons and change the threshold voltage of the first memory cell to a programmed state; and

applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons and deter change in the threshold voltage of the second memory cell.

Claim 2 (original): The method of claim 1 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is in a range of about 10 volts to about 10.5 volts, and the third voltage is about –1.5 volts.

Claim 3 (currently amended): The method of claim 1 wherein the generating ~~establishing~~ step comprises applying a fourth voltage and a fifth voltage to, respectively, source and drain regions defining the channels of the first and second memory cells, the fourth voltage being applied through a common ground line and the fifth voltage being applied through a bit line.

Claim 4 (original): The method of claim 3 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is about 10.5 volts, the third voltage is about –1.5 volts, the fourth voltage is about 0 volts, and the fifth voltage is about 4.5 volts.

Claim 5 (currently amended): The method of claim 1 wherein the generating ~~establishing~~ step comprises applying a fourth voltage and a fifth voltage to, respectively, source and drain regions defining the channels of the first and second memory cells, the fourth voltage being applied through a virtual ground line and the fifth voltage being applied through a bit line.

Claim 6 (original): The method of claim 5 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is about 10 volts, the third voltage is about –1.5 volts, the fourth voltage is about 0 volts, and the fifth voltage is about 4.5 volts.

Claims 7-17 (canceled)

Claim 18 (original): A memory comprising:

a memory array having a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a channel and being programmable using channel hot electron injection;

a voltage source for applying a first voltage to the channels;

a voltage source for establishing a voltage differential across the respective channels of at least a first and a second of the memory cells, the potential differential being sufficient to generate channel hot electrons in the respective channels thereof;

a voltage source for applying a second voltage to the gate of the first memory cell, the second voltage having a polarity and magnitude relative to the first voltage sufficient to attract the hot electrons and change the threshold voltage of the first memory cell to a programmed state; and

a voltage source for applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons and deter change in the threshold voltage of the second memory cell.

Claims 19-22 (canceled)

Claim 23 (new): A NOR-type memory integrated circuit comprising:

a plurality of word select lines;

a plurality of bit lines;

a plurality of source lines;

a memory array having a plurality of adjustable threshold voltage memory transistors, each being programmable using channel hot electron injection and having a source coupled to one of the source lines, a drain coupled to one of the bit lines, a floating gate overlying a channel defined in a substrate body region between the source and the drain, and a control gate overlying the floating gate and coupled to one of the word select lines;

a voltage source for applying a body voltage to the substrate body regions containing the channels;

a voltage source for applying a source voltage to the sources of at least a first and a second of the memory transistors via a common one of the source lines;

a voltage source for applying a drain programming voltage to the drains of the first and second memory transistors via a common one of the column lines, the source and drain programming voltages being sufficient to generate channel hot electrons in the respective channels of the first and second memory transistors;

a voltage source for applying a select voltage to the gate of the first memory transistor via a first one of the word select lines, the select voltage having a polarity and magnitude relative to the body voltage sufficient to attract the hot electrons of the first memory transistor and change the threshold voltage thereof to a programmed state; and

a voltage source for applying an unselect voltage to the gate of the second memory cell via a second one of the word select lines, the unselect voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons of the second memory transistor and deter change in the threshold voltage thereof.

Claim 24 (new): The memory integrated circuit of claim 23 wherein:

the body voltage is about 0 volts;

the source voltage is about 0 volts;

the drain programming voltage is about 4.5 volts;

the select voltage is in a range of about 10 volts to about 10.5 volts; and

the unselect voltage is about −1.5 volts.

Claim 25 (new): A virtual ground-type memory integrated circuit comprising:

a plurality of word select lines;

a plurality of column lines;

a memory array having a plurality of adjustable threshold voltage memory transistors, each being programmable using channel hot electron injection and having a source coupled to one of the column lines, a drain coupled to an adjacent one of the column lines, a floating gate

overlying a channel defined in a substrate body region between the source and the drain, and a control gate overlying the floating gate and coupled to one of the word select lines;

a voltage source for applying a body voltage to the substrate body regions containing the channels;

a voltage source for applying a reference voltage to the sources of at least a first and a second of the memory transistors via a first one of the column lines;

a voltage source for applying a programming voltage to the drains of the first and second memory transistors via a second one of the column lines adjacent the first column line, the reference and programming voltages being sufficient to generate channel hot electrons in the respective channels of the first and second memory transistors;

a voltage source for applying a select voltage to the gate of the first memory transistor via a first one of the word select lines, the select voltage having a polarity and magnitude relative to the body voltage sufficient to attract the hot electrons of the first memory transistor and change the threshold voltage thereof to a programmed state; and

a voltage source for applying an unselect voltage to the gate of the second memory cell via a second one of the word select lines, the unselect voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons of the second memory transistor and deter change in the threshold voltage thereof.

Claim 26 (new): The memory integrated circuit of claim 25 wherein:

the body voltage is about 0 volts;

the reference voltage is about 0 volts;

the programming voltage is about 4.5 volts;

the select voltage is in a range of about 10 volts to about 10.5 volts; and

the unselect voltage is about –1.5 volts.